

AMENDMENTS TO THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application.

- 1                   1. (currently amended) ~~An A system interface between a master and one or~~  
2 ~~more slave modules~~ comprising:  
3                   a master;  
4                   a slave ~~having a set of addressable registers including egress mailbox registers,~~  
5 ~~ingress mailbox registers, and indirect access address registers;~~  
6                   a direct memory access (DMA) engine ~~coupled to a the master by a first bus~~  
7 ~~and to the slave by a second bus, with the second bus comprising:~~  
8                   a Packet Voice Data Module (PVDM) having a set of bi-directional data lines  
9 inputs/outputs configured as an interface between a master device coupled to a DMA engine  
10 and a slave device having a set of addressable registers including egress mailbox registers,  
11 ingress mailbox registers, and indirect access address registers, with the interface comprising  
12 for transmitting data between the slave and the DMA engine;  
13                   a set of master address ~~lines~~ inputs configured to couple the PVDM to the  
14 DMA engine, with the master address for transmitting address data from the DMA engine to  
15 the slave;  
16                   a master data strobe input configured to couple the PVDM to the DMA  
17 engine, with the master data strobe for strobing data;  
18                   a master read/write signal input configured to couple the PVDM to the DMA  
19 engine, with master read/write signal for indicating whether data is to be read from or written  
20 to the slave;  
21                   a set of slave select signal inputs configured to couple the PVDM to the DMA  
22 engine, with slave select signals for selecting one of a plurality of slaves ~~connected to the~~  
23 ~~second bus;~~  
24                   a slave wait signal output configured to couple the PVDM to the DMA engine,  
25 with the slave wait signal asserted by a slave to delay a data transfer;  
26                   a slave reset signal input configured to couple the PVDM to the DMA engine,  
27 with the slave reset signal resetting the slave when asserted;

28                   a clock ~~output~~ signal line output configured to couple the PVDM to the DMA  
29 engine and to receive a clock signal; [,]and

30                   a clock ~~input~~ signal line input configured to couple the PVDM to the DMA  
31 engine and to receive a clock input signal[;]

32                   ~~where the DMA engine performs direct data transfers to the slave by asserting~~  
33 ~~a slave select signal to the slave and transferring data over the set of bi-directional data lines~~  
34 ~~to the slave egress or ingress data registers and performs indirect data transfers to slave~~  
35 ~~memory by writing address data over the set of bi-directional data lines to the indirect address~~  
36 ~~register of the slave and where the slave utilizes its own memory map and the address data to~~  
37 ~~transfer data between a location indicated by the address data and the DMA engine.~~

1                   2. (currently amended) The system interface of claim 1 further comprising a  
2 where the DMA engine configured to perform direct data transfers to the slave by asserting a  
3 slave select signal to the slave and to transfer data to the slave egress or ingress data registers  
4 and to perform indirect data transfers to slave memory by writing address data to the indirect  
5 address register of the slave and to negotiate ~~negotiates~~ with a slave to implement either an  
6 asynchronous, synchronous, or source synchronous data transfer.

1                   3. (currently amended) The system interface of claim 2 ~~claim 1~~ with where  
2 the DMA engine configured to negotiate ~~negotiates~~ with all slaves during reset to determine a  
3 the maximum bus width available to transfer data.

1                   4. (currently amended) The system interface of claim 1 further comprising  
2 where:

3                   ~~the a slave including a includes~~ status register and a message signal interrupt  
4 (MSI) register; and

5                   where the slave is configured to utilize its own memory map and the address  
6 data to transfer data between a location indicated by the address data and the DMA engine  
7 and to assert ~~asserts~~ a bit in the status register to indicate it is ready for a transaction and  
8 where the DMA engine is configured to assert ~~asserts~~ a bit in the MSI register to indicate  
9 when a transaction is complete.

1                   5. (currently amended) A method ~~for allowing a DMA engine to provide~~  
2 ~~access to a plurality of slave devices to multiple masters, the protocol, implemented by~~  
3 ~~hardware and software on the DMA engine, the master, and the slave devices, comprising the~~  
4 ~~steps of:~~

5                   to implement a direct message transfer to a slave:

6                   accessing a slave status register to read a direct message ready  
7 status bit which is set when the slave is ready to transfer data;  
8 transferring message data using ~~a~~ the DMA engine and a slave mailbox  
9 register if the direct message ready status bit is set;

10                  setting ~~a~~ an message transfer complete status interrupt at the  
11 slave to indicate when the transfer of the message is complete; and  
12 to implement an indirect data transfer to the memory space of a slave device:

13                  accessing a slave status register to read an indirect message  
14 ready status bit which is set when the slave is ready to transfer data;  
15 transferring address data using the DMA engine and slave  
16 indirect address mailbox register if the indirect message ready status  
17 bit is set;

18                  setting an indirect transfer message interrupt bit at the slave to  
19 initiate the indirect transfer;

20                  transferring message data between the DMA engine and slave  
21 mailbox registers if the indirect message ready status bit is set, where  
22 the slave utilizes its own memory map and the address data to transfer  
23 data between a location indicated by the address data and the DMA  
24 engine; and

25                  setting ~~a~~ an message transfer complete status interrupt at the  
26 slave to indicate when the transfer of the message is complete.

1                   6. (currently amended) The method of claim 5 further comprising ~~the step of:~~  
2 negotiating with all the slaves to implement either an asynchronous,  
3 synchronous, or source synchronous data transfer.

1                   7. (currently amended) The method of claim 5 further comprising ~~the step of:~~

2 starting the bus upon reset at a fixed bus-width and then negotiating with all  
3 the slaves to implement acceptable bus bit-width.

1 8. (currently amended) A system ~~allowing a DMA engine to provide access~~  
2 ~~to a plurality of slave devices to multiple masters, the protocol, implemented by hardware and~~  
3 ~~software on the DMA engine, the master, and the slave devices, said system~~ comprising:

4 means for implementing a direct message transfer to a slave device including:

5 means for accessing a slave status register to read a direct message ready  
6 status bit which is set when the slave is ready to transfer data;

7 means for transferring message data using ~~a~~ the DMA engine and a slave  
8 mailbox register if the direct message ready status bit is set;

9 means for setting ~~a~~ ~~an~~ message transfer complete status interrupt at the slave  
10 to indicate when the transfer of the message is complete; and

11 means for implementing ~~implement~~ an indirect data transfer to the memory  
12 space of a slave device including:

13 means for accessing a slave status register to read an indirect message ready  
14 status bit which is set when the slave is ready to transfer data;

15 means for transferring address data using the DMA engine and slave indirect  
16 address mailbox register if the indirect message ready status bit is set;

17 means for setting an indirect transfer message interrupt bit at the slave to  
18 initiate the indirect transfer;

19 means for transferring message data between the DMA engine and slave  
20 mailbox registers if the indirect message ready status bit is set, where the slave utilizes its  
21 own memory map and the address data to transfer data between a location indicated by the  
22 address data and the DMA engine; and

23 means for setting ~~a~~ ~~an~~ message transfer complete status interrupt at the slave  
24 to indicate when the transfer of the message is complete.

1 9. (Original) The system of claim 8 further comprising:

2 means for negotiating with all the slaves to implement either an asynchronous,  
3 synchronous, or source synchronous data transfer.

1 10. (Original) The system of claim 8 further comprising:

- 2 means for starting the bus upon reset at a fixed bus-width and then negotiating
- 3 with all the slaves to implement acceptable bus bit-width.
- 1

1                    11. (currently amended) An apparatus ~~A slave device for allowing a DMA engine to~~  
2 ~~provide access by multiple masters, said slave device~~ comprising:

3                    a slave status register accessible ~~aeessed~~ to read a direct message ready status bit  
4 which is set when the slave is ready to transfer data directly and accessible ~~aeessed~~ to read an  
5 indirect message ready bit which is set when the slave is ready to transfer data indirectly;

6                    a slave mailbox register configured to transfer ~~for transferring~~ direct message data  
7 using ~~a the~~ DMA engine if the direct message ready status bit is set and with the slave mailbox  
8 registers used for transferring message data using the DMA engine if an indirect message ready  
9 status bit is set;

10                   a message transfer complete status interrupt at the slave configured ~~that is set~~ to  
11 indicate when the transfer of the message is complete;

12                   a slave indirect address mailbox register configured to transfer ~~for transferring~~  
13 address data using the DMA engine if the indirect message ready status bit is set;

14                   an indirect transfer message interrupt bit at the slave configured to ~~which is set to~~  
15 initiate the indirect transfer; and

16                   a slave memory map configured for use ~~used~~ with the address data to transfer data  
17 between a location indicated by the address data and the DMA engine.